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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,393	08/30/2001	Kie Y. Ahn	303.678US4	9764

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EXAMINER	
DANG, PHUC T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,393	AHN ET AL.	
	Examiner	Art Unit	
	PHUC T DANG	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Pre-Amnedment filed August 30, 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *67-77* is/are allowed.

6)☒ Claim(s) *41-44,47-51,55-59 and 62-66* is/are rejected.

7)☒ Claim(s) *44-46,52-54 and 60* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This application is a divisional of U.S. Patent Application No. 09/514,629, filed on February 28, 2000.

Pre-Amendment

2. Pre-Amendment filed on August 30, 2001 has been entered and made of record as Paper No. 3.

In Pre-Amendment, applicants canceled claims 1-40 and claims 31-77 are remained for examination.

Oath/Declaration

3. The oath/declaration filed on August 30, 2001 is acceptable.

Information Disclosure Statement

4. The office acknowledges receipt of the following items from the applicant:

Information Disclosure Statement (IDS) filed on August 30, 2001.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Lowrey et al. (U.S. Patent No. 5,057,449).

Okazawa teaches a circuit on a single substrate, comprising:

a logic device (110, Fig. 1), wherein the logic device further includes a transistor with a dielectric layer (42, Fig. 3A) having a first thickness including a top layer (43, Fig. 3A) which exhibits a high resistance to oxidation at high temperatures (1000°C); and

a memory device (210, Fig.1) coupled to the logic device, wherein the memory device further includes a transistor with a dielectric layer having a second thickness greater than the dielectric layer of the first thickness but less than 12 nanometers [col. 5, lines 37-42].

Okazawa discloses all the features of the claimed invention as discussed above, but does not disclose the dielectric layer of the second thickness is formed entirely of silicon dioxide (SiO_2).

Lowrey et al., however, disclose the dielectric layer of the second thickness is formed entirely of silicon dioxide (SiO_2) [col. 3, lines 49-52].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Lowrey et al. to Okazawa discussed above such that

the dielectric layer of the second thickness is formed entirely of silicon dioxide for a purpose of improving electrical and physical characteristics over silicon dioxide.

6. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view of Lowrey et al., and further in view of Cavins et al. (U.S. Patent No. 5,731,238).

Okazawa and Lowrey et al. disclose all the features of the claimed invention as discussed above, but do not disclose the dielectric layer having a first thickness includes a dielectric layer of less than 7 nanometers, wherein the dielectric layer has a bottom layer of silicon dioxide ($Si0_2$), and wherein the top layer is silicon nitride (Si_3N_4).

Cavins et al., however, disclose the dielectric layer having a first thickness includes a dielectric layer of less than 7 nanometers, wherein the dielectric layer has a bottom layer of silicon dioxide ($Si0_2$), and wherein the top layer is silicon nitride (Si_3N_4) [col. 5, lines 58-64].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Lowrey et al. to Okazawa discussed above such that the dielectric layer having a first thickness includes a dielectric layer of less than 7 nanometers, wherein the dielectric layer has a bottom layer of silicon dioxide ($Si0_2$), and wherein the top layer is silicon nitride (Si_3N_4) [col. 5, lines 58-64] in the logic device transistor circuit.

7. Claims 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view of Lowrey et al., and further in view of Liu et al. (U.S. Patent No. 5,257,095).

Okazawa and Lowrey et al. disclose all the features of the claimed invention as discussed above, but do not disclose the logic device transistor and the memory device transistor both

include a gate formed from boron doped polysilicon, and wherein the top layer of the dielectric layer having a first thickness exhibits a strong resistance to boron penetration at high temperatures (300°C).

Liu et al., however, disclose the logic device transistor and the memory device transistor both include a gate formed from boron doped polysilicon, and wherein the top layer of the dielectric layer having a first thickness exhibits a strong resistance to boron penetration at hightemperatures (300°C) [col. 4, lines 4-10 and col. 10, lines 66-68].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Lowrey et al. to Okazawa discussed above such that the dielectric layer having a first thickness includes a dielectric layer of less than 7 nanometers, wherein the dielectric layer has a bottom layer of silicon dioxide ($Si0_2$), and wherein the top layer is silicon nitride (Si_3N_4) for a purpose of increasing the capacitance value of the integrated circuit.

8. Claims 47 and 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. patent No. 6,091,109) and further in view of Liu et al. (U.S. Patent No. 5,257,095).

Okazawa discloses a system on a chip, comprising:a logic device (110, fig. 1), wherein the logic device further includes a transistor with a dielectric layer (42, Fig. 3A) having a first thickness including a top layer which exhibits a high resistance to oxidation at high temperatures; and

a memory device (210,Fig. 1) coupled to the logic device, wherein the memory device further includes a transistor with a dielectric layer having a second thickness [col. 5, lines 37-42].

Okazawa discloses all the features of the claimed invention as discussed above, but does not disclose the transistor with a dielectric layer having a first thickness of less than 7 nanometers.

Liu et al., however, disclose the transistor with a dielectric layer having a first thickness of less than 7 nanometers [col. 10, lines 66-68].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu et al. to Okazawa discussed above such that the dielectric layer having a first thickness includes a dielectric layer of less than 7 nanometers for a purpose of increasing the capacitance value of the integrated circuit.

Okazawa and Liu et al. disclose all the features of the claimed invention as discussed above, but do not disclose the dielectric layer having a second thickness greater than the dielectric layer of the first thickness but less than 12 nanometers.

Hasegawa, however, disclose the dielectric layer having a second thickness greater than the [illegible] but less than 12 nanometers [col. 8, lines 31-33].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Hasegawa to Okazawa and Liu et al. discussed above such that the dielectric layer having a second thickness greater than the dielectric layer of the first thickness but less than 12 nanometers for a purpose of increasing the capacitance value of the integrated circuit.

Regarding claims 49-51, Okazawa discloses all the features of the claimed invention as discussed above, but does not disclose the logic device transistor and the memory device transistor both include a gate formed from boron doped polysilicon, and wherein the top layer of the dielectric layer having a first thickness exhibits a strong resistance to boron penetration at high temperatures (300 and 800 degrees Celsius).

Liu et al., however, disclose the logic device transistor and the memory device transistor both include a gate formed from boron doped polysilicon, and wherein the top layer of the dielectric layer having a first thickness exhibits a strong resistance to boron penetration at high temperatures (300 and 800 degrees Celsius) [col. 10, lines 4-11].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu et al. to Okazawa and Hasegawa discussed above such that the logic device transistor and the memory device transistor both include a gate formed from boron doped polysilicon, and wherein the top layer of the dielectric layer having a first thickness exhibits a strong resistance to boron penetration at high temperatures for a purpose of providing for the reliable fabrication of an enhanced integrated circuit.

0 Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view of Hasegawa and Liu et al., and further in view of Cavins et al. (U.S. Patent No. 5,741,238).

Okazawa, Hasegawa and Liu et al. disclose all the features of the claimed invention as discussed above, but do not disclose the dielectric layer having a first thickness includes a dielectric layer having a bottom layer of silicon dioxide (SiO_2), and wherein the top layer is silicon nitride (Si_3N_4).

Cavins, however, discloses the dielectric layer having a first thickness includes a dielectric layer having a bottom layer of silicon dioxide (SiO_2), and wherein the top layer is silicon nitride (Si_3N_4) [col. 5, lines 58-64].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Hasegawa to Okazawa and Liu et al. discussed above such that the dielectric layer having a first thickness includes a dielectric layer having a bottom layer of silicon dioxide (SiO_2), and wherein the top layer is silicon nitride (Si_3N_4) for a purpose of increasing the capacitance value of the integrated circuit.

10. Claims 55-56 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Liu et al. (U.S. Patent No. 5,256,095).

Okazawa discloses a circuit on a single substrate, comprising:

a logic device (110, Fig. 1), wherein the logic device includes a transistor with a dielectric layer (42, Fig. 3A) including a first dielectric layer of a first thickness;

a top layer (43, Fig. 3A) which exhibits a high resistance to oxidation at high temperatures; and

a memory device (210, Fig. 1)coupled to the logic device, wherein the memory device further includes a transistor with a second dielectric layer having a second thickness greater than the dielectric layer of the first thickness.

Okazawa discloses all the features of the claimed invention as discussed above, but does not disclose the first dielectric layer of a thickness less than 5 nanometers.

Liu et al., however, disclose the first dielectric layer of a thickness less than 5 nanometers [col. 10, lines 66-68].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu et al. to Okazawa discussed above such that the first dielectric layer of a thickness less than 5 nanometers for a purpose of requiring lower process temperature.

Regarding claim 56, Liu et al. disclose the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu et al. to Okazawa discussed above such that the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm) for a purpose of requiring lower process temperature.

Regarding claim 61, Liu et al. disclose the top layer exhibits a high resistance to boron penetration at high temperatures [col. 10, lines 66-68].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu et al. to Okazawa discussed above such that the top layer exhibits a high resistance to boron penetration at high temperatures for a purpose of requiring lower process temperature.

11. Claims 57 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view of Liu et al., and further in view of Cavins et al. (U.S. patent No. 5,731,239).

Okazawa and Liu et al. disclose all the features of the claimed invention as discussed above, but do not disclose the first dielectric layer of a first thickness includes silicon dioxide (SiO_2) and the top layer includes silicon nitride (Si_3N_4).

Cavins et al., however, disclose the first dielectric layer of a first thickness includes silicon dioxide (SiO_2) and the top layer includes silicon nitride (Si_3N_4) [col. 5, lines 58-64].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Cavins et al. to Okazawa and Liu et al. discussed above such that the first dielectric layer of a first thickness includes silicon dioxide (SiO_2) and the top layer includes silicon nitride (Si_3N_4) for a purpose of increasing the capacitance value of the integrated circuit.

12. Claims 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view of Liu et al., and further in view of Lowrey et al. (U.S. patent No. 5,057,449).

Okazawa and Liu et al. disclose all the features of the claimed invention as discussed above, but do not disclose the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (Si02).

Lowrey et al. however, disclose the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (Si02) [col. 3, lines 49-52].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Lowrey et al. to Okazawa and Liu et al. discussed above such that the second dielectric layer of a second thickness includes a dielectric layer

formed entirely of silicon dioxide (Si02) for a purpose of improving electrical and physical characteristics over silicon dioxide.

13. Claims 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view of Liu et al., and further in view of Hasegawa (U.S. patent No. 6,091,109).

Okazawa and Liu et al. disclose all the features of the claimed invention as discussed above, but do not disclose the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

Hasegawa, however, discloses the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers [col. 8, lines 31-33].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Hasegawa to Okazawa and Liu et al. discussed above such that the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers for a purpose of improving the desired characteristics and properties of the thickness of the gate oxide.

14. Claims 62-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Liu et al. (U.S. Patent No. 5,257,095).

Okazawa discloses a circuit on a single substrate, comprising:

a logic device, wherein the logic device includes a transistor with a dielectric layer;

a top layer which exhibits a high resistance to boron penetration at high temperatures; and a memory device coupled to the logic device, wherein the memory device further includes a

transistor with a second dielectric layer having a second thickness greater than the dielectric layer of the first thickness [col. 5, lines 37-42].

Okazawa discloses all the features of the claimed invention as discussed above, but does not disclose the dielectric layer of a first thickness less than 5 nanometers.

Liu et al., however, disclose the dielectric layer of a first thickness less than 5 nanometers [col. 10, lines 66-68].

Regarding claim 63, Liu et al. disclose the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm) [col. 10, lines 66-col. 11, lines4].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu et al. to Okazawa discussed above such that the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm) for a purpose of requiring lower process temperature.

15. Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view of Liu et al., and further in view of Cavins et al. (U.S. Patent No. 5,731,238).

Okazawa and Liu et al. disclose all the features of the claimed invention as discussed [illegible] dielectric layer of a first thickness includes silicon dioxide (SiO2) and the top layer includes silicon nitride (Si3N4).

Cavins et al., however, disclose the first dielectric layer of a first thickness includes silicon dioxide (SiO2) and the top layer includes silicon nitride (Si3N4) [col. 5, lines 58-64].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Cavins et al. to Okazawa and Liu et al. discussed

above such that the first dielectric layer of a first thickness includes silicon dioxide (SiO2) and the top layer includes silicon nitride (Si3N4) for a purpose of increasing the capacitance value of the integrated circuit.

16. Claim 65 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view of Liu et al.. and further in view of Lowey et al. (U.S. Patent No. 5,057,449).

Okazawa and Liu et al. disclose all the features of the claimed invention as discussed above, but do not disclose the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (Si02) [col. 3, lines 39-42].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Lowrey et al. to Okazawa and Liu et al. discussed above such that the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (Si02) for a purpose of increasing the capacitance value of the integrated circuit.

17. Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view of Liu et al., and further in view of Hasegawa (U.S. Patent No. 6,091,109).

[illegible] features of the claimed invention as discussed above, but do not disclose the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

Hasegawa, however, discloses the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers [col. 8, lines 31-33].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Hasegawa to Okazawa and Liu et al. discussed above such that the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers for a purpose of improving the desired characteristics and properties of the thickness of the gate oxide.

Allowable Subject Matter

18. Claims 67-77 would be allowed.

The following is a statement of reason for the indication of allowable subject matter:

Claims 67-77 are considered allowable since the prior art of record and the considered pertinent to the applicant's disclosure does not teach or suggest the claimed invention. Okazawa (U.S. Patent No. 4,700,212) and the other references, taken individually or in combination, do not teach the claimed invention having a silicon nitride top layer which exhibits a high resistance to oxidation at high temperature as disclosed in claim 67 and a layer of a silicon nitride top layer of approximately a third of the first thickness which exhibits a high resistance to oxidation at high temperatures as disclosed in claim 73 and the step of forming a pair gate oxides on the first [illegible] first thickness of less than 5 nanometers by krypton plasma generated atomic oxygen at approximately 400 degrees Celsius as disclosed in claim 77.

Claims 45-46, 52-54, and 60 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art of record failed to suggest the dielectric layer of a first thickness having a top layer which exhibits a high resistance to

oxidation at high temperatures includes a top silicon nitride which comprises approximately a third of the first thickness of the dielectric layer as disclosed in claims 4, 52 and 60.

Claims 46 depends on claim 45 and claims 53-54 depend on claim 52, then, they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is 703-305-1080. The examiner can normally be reached on 8:00 am-5:00 pm.

20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-5841 for After Final communications.

21. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Phuc T. Dang PD

Examiner

Art Unit 2818

PHUC T DANG
EXAMINER

August 23, 2002